A LOW NOISE SINGLE-ENDED GaAs SCHOTTKY FET AMPLIFIER FOR A 14 GHz SATELLITE COMMUNICATION APPLICATION

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ABSTRACT

A 14.0 - 14.5 GHz amplifier consisting of a cascade of three single-ended stages which realizes a noise figure of 3.5 dB and a gain of 17 dB has been designed. This has been achieved with a new design technique which is tolerant of changes in FET S-parameters and yet capable of extracting the maximum performance of the device. Results on a 10 GHz amplifier designed with the above technique will also be given.

Design Approach

Many designers have recognized the value of using a single-ended input module (as opposed to a balanced configuration) to set the noise figure of a low noise amplifier.[1,2] There are two practical advantages to this method. Firstly, in a single-ended module only one FET sets the noise figure and thus the highest performance device may be chosen for the input stage. Secondly, in a single-ended circuit alignment of the input and output matching structures can proceed on the basis of direct return loss measurements without having to de-embed the transformation that couplers produce. Additionally, direct measurements of the S-parameters of a single-ended module provides necessary information in the early stages of amplifier development when correlation between the performance of an amplifier and computer predictions are vital for analyzing the circuit. A disadvantage of the single-ended input approach is that an input isolator is required to reduce input VSWR, resulting in increased size and weight.

Although a single-ended input stage is commonly employed, succeeding stages are often of balanced design to insure low VSWR and thus minimal interaction between cascaded stages. Single-ended designs necessarily exhibit high input VSWR when designed for minimum noise figure. Thus cascaded single-ended stages offer the potential for interaction (or mismatch) between stages which may result in severe gain ripple and gain variation over temperature. One may design output to input interstage matching structures to control this problem. However, such designs tend to be highly sensitive to minor device and circuit fabrication variations — both of which may be expected at 14 GHz. Therefore, the approach taken here is to design the output circuit to provide very low VSWR (high return loss) such that a well controlled source impedance will be presented to successive single-ended input circuits. It is noted that this approach is valid only for narrow bandwidth applications. Wide band designs generally require mismatch of the output to achieve gain flatness.

The amplifier described herein represents an attempt to deal with the problems of cascading several single-ended stages. In particular, the questions of amplifier stability and definition of a ripple-free, well behaved band pass gain over temperature are addressed. Identical single-ended low noise circuits were used in order to obtain the lowest amplifier noise figure and the highest possible module yield. This circuit commonality allows test of each stage and thus identification of the lowest noise figure to precede the higher noise figure units. The approach assumes a significant statistical variation in the device noise figures will be experienced.

Although first stage noise figure is dominant, noise figure contributions of the second stage module are also important when gain per stage is low (6 dB in this case). Choosing a single-ended over a balanced second stage module (assuming a single-ended second stage noise figure of 3.0 dB at 14.5 GHz versus a 3.6 dB value typical of a balanced low noise module and a 2.8 dB value characteristic of the input low noise single-ended module) would cause a 0.15 dB lower amplifier noise figure at 14.5 GHz. Furthermore, as the output of each low noise module is aligned for greater than 20 dB return loss in band, the low noise module following it looks back into a 50 ohm source which is the condition for low noise operation in this technique. Since most fabricated modules can be placed somewhere in the amplifier chain, this method results in most of the modules (about 90%) being placed in completed amplifiers and suggests the ease of large scale production. The single-ended amplifier approach is also advantageous whenever power consumption must be minimized as it requires about 1/2 that of its typical low noise balanced counterpart.

Design Goals

The foremost goal here was to develop the lowest noise figure amplifier possible in the 14.0-14.5 GHz band. Towards this end, the designing was constrained to satisfy four criteria: 1) A circuit flexible enough that maximum amplifier performance could be achieved without major alignment, even if the FETs were to vary slightly in S-parameters due either to changes in FET characteristics between lots or to slight variations in the bonding techniques employed; 2) A single-ended circuit able to provide output return loss of greater than 20 dB in band. This provides the second stage module with a 50 ohm source required to minimize noise figure in this technique, and allows $|S_{22}|$ to be small over the temperature range minimizing the possibility of non-monotonic changes in the gain bandpass behavior over temperature. The output return loss requirement should enhance amplifier stability and because of the narrow bandwidth of the match should generate a bandpass in which gain is higher in-band than out-of-band; 3) Alignment of the circuit for maximum performance of the single-ended circuit should be achieved by controlling the length of open circuited shunt stubs only; 4) The circuit must be capable of being assembled in a highly repeatable fashion. This is a necessary condition for any production circuit and it is an important consideration in Ku-band where slight assembly changes can greatly affect performance.

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Realization of the Single-Ended Circuit

The circuit was designed to use the NEC 388 GaAs FET chip which possesses a $1/2\mu$ gate length.[3] Data on several FET devices was taken to determine the match for minimum noise figure (Γ_{on}) and to acquire typical S-parameters. The measurement fixture used was designed to incorporate bias tees invisible to the FET from 12 to 16 GHz. To calculate Γ_{on} the seven source method of determining minimum noise figure was used where sources are presented to a FET whose output is tuned to 50 ohms and the noise figure obtained are recorded.[4] Our computer program using a least squares method derived the noise parameters r_n, Γ_{on} and NF_{min} from this data. The computer predicted Γ_{on}, while smaller in magnitude, did not differ significantly from the Γ_{source} measured under minimum noise measure conditions.

Numerous data files containing various Γ_{on}, S_{11} and S_{22} values versus frequency were compiled to represent the likely variations of these quantities. Figure 1 shows two curves each for Γ_{on} and S_{22} versus frequency between 13 and 16 GHz. The region between each of these sets of curves represents the likely excursion of Γ_{on} and S_{22} from their typical values (dashed curves). The single-ended 14 GHz low noise amplifier circuit design tolerates parameter variation within these regions. Input and output matching networks of the 14.0 - 14.5 GHz single-ended amplifier are shown in Figure 2. Each network consists of five microstrip transmission lines symmetrically disposed around the FET. The two sets of opposed open and short circuited shunt stubs (OCSS and SCSS) allow the circuit to tolerate variations in S-parameters merely by properly adjusting their lengths relative to one another.

1. The optimum match for noise figure Γ_{on} and the output reflection coefficient S_{22} for a NEC 388 chip GaAs FET.
Values are given from 13-16 GHz.
2. Schematic circuit diagram of the LN single-ended 14.0-14.5 GHz amplifier. Also shown is the optional output filter. All lengths l are less than 0.60λ.
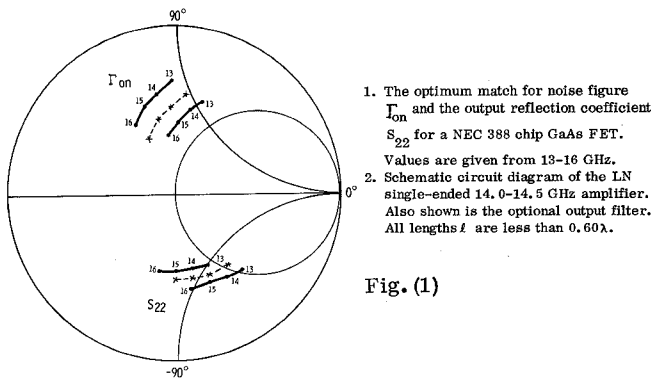
Fig. (1)

Length adjustment of the OCSS's is used to cover a region about the desired reflection coefficients to be matched. For the output matching circuit S_{22} is matched to a 50 Ω source.

For the input matching circuit a 50Ω source is mapped into a desired Γ_{on} value needed to obtain the minimum NF. Figure 3 demonstrates the behavior of the Γ_{on} match as the OCSS's are varied in length. Depending on their lengths, they appear inductive or capacitive to the matching circuit and are entirely reactive. One can show that a purely reactive element conformally maps on the Smith Chart to form circular contours.[5] The contours for the two OCSS's in the circuit (labeled 2 and 5 for those circuit elements) are shown

in the figure. Contour 2 is obtained by maintaining the length of element 5 at its initial value and varying the length of element 2. Contour 5 is similarly generated. The intersection of these two contours locates the initial unaligned Γ_{on} value. Impedance coverage about that point is delineated by the contours emanating from that point. All calculations in Figure 3 are for 14.250 GHz.
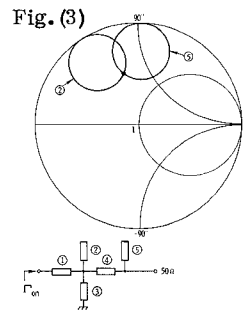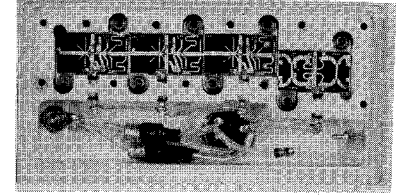
Fig. (3)   Fig. (4)

3. Variation of Γ_{on} match with varying elemental lengths of the OCSS's 2 and 5 shown in the inset. Values are for 14.25 GHz.
4. Thin film four stage LN amplifier with three single-ended stages followed by a balanced stage.

Figure 4 shows an aligned four stage amplifier composed of three cascaded single-ended stages followed by a balanced gain unit. Several of the low impedance stubs have been realized by the use of two higher impedance lines in parallel. This topology allows straightforward alignment for optimum noise and output match, but it also has the disadvantage of being relatively inefficient in the utilization of substrate area.

It is difficult, for example, to accommodate two such topologies in a balanced configuration in a width less than $\lambda/2$ (to avoid cavity moding).

The design technique has also been used at 10 GHz for a single-ended circuit which is placed in an amplifier consisting of two single-ended cascaded stages followed by one balanced stage. For amplifiers whose bandwidth is desired to be in excess of 3.5%, it has been experimentally determined that appropriate adjustment of the impedance of the series transmission lines must occur to maintain gain flatness. Data on both the 10 GHz and 14 GHz amplifiers will be given below.
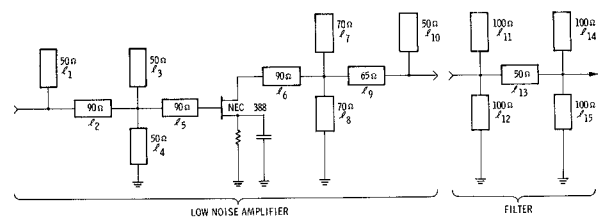
Fig. (2)

Results

Figure 5 shows noise figure versus frequency on a 14 - 14.5 GHz four stage amplifier composed of three single-ended stages with an output balanced stage (Figure 4). The response which shows a minimum noise figure near midband and increases on either side suggests the sensitivity of the match to Γ_{on}. The noise figure at 14.5 GHz of the three single-ended modules which comprise this amplifier was calculated from the measured system noise figure to be 2.50 dB, 2.56 dB, and 2.67 dB for, respectively, the input, second and third modules. The spread in module noise figure was taken advantage of by cascading the modules in order of increasing noise figure. Output return loss of several single-ended modules is shown in Figure 6. 20 dB return loss or better is achieved across the band, indicating that it was possible to realize a good match to the FET by varying the lengths of the OCSS's on the output network.
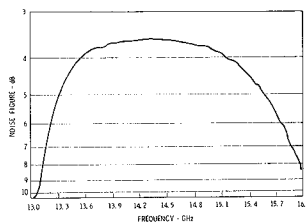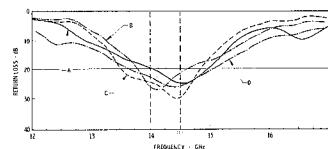
Fig. (5)

Fig. (6)

Fig. (8)

Fig. (9)

5. Noise figure versus frequency for a 14.0-14.5 GHz four stage amplifier consisting of three single-ended stages and one following balanced stage. NF accuracy is better than ± 0.1 dB over 13.5-15.0 GHz.
6. Output return loss versus frequency for four separate LN single-ended stages labeled A, B, C and D. V_{DS} = 5.0 V. All units were aligned for NF and S_{22}.

8. Gain versus frequency in-band from 14.00 - 14.50 GHz for a three stage LN amplifier consisting of three single-ended modules. Parameterization in terms of the ambient temperature is indicated on the curves.
9. Noise figure and gain versus frequency for a 10 GHz LN amplifier with two single-ended stages and three balanced stages.

The gain response of three single-ended stages, cascaded in a three stage amplifier housing, each aligned for noise figure and output return loss, but prior to amplifier alignment is shown by the solid line in Figure 7a. The lack of in-band gain ripple is attributable to the high output return loss of each module. In-band gain roll-off is about 1 dB. Gain flatness was easily achieved by realignment of the input matching structure of the third single-ended module (far enough along in the cascade to not degrade noise figure). Removal of an undesirable out-of-band gain peak at about 12 GHz was achieved by the addition of the 12 GHz reject filter section on the third single-ended module. The filter is included for optional use on the output of every single-ended module; its circuit block diagram is shown in the right hand portion of Figure 2. In Figure 7a the dotted line represents the gain achieved once alignment has been completed for in-band gain flatness, noise figure, and out-of-band gain. Aligning the amplifier for noise figure typically results in an 0.05 to 0.10 dB improvement from the turn-on noise figure. The gain response of a four stage (three single-ended stages and an output balanced stage) amplifier before and after similar alignment is exhibited in Figure 7b where the dotted line indicates gain achieved after alignment.
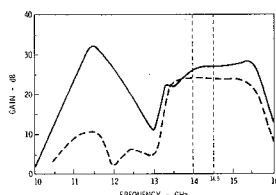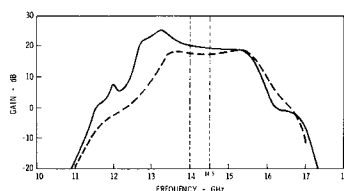

Fig. (7a)

Fig. (7b)

7. a) Gain versus frequency for a three stage LN amplifier containing three single-ended modules. Solid and dashed lines are, respectively, before and after alignment for NF and G. (A filter is present for the dashed curve.) b) Gain versus frequency for a four stage LN amplifier containing three single-ended modules followed by one balanced unit. Solid and dashed lines are, respectively, before and after alignment for NF and G. (A filter is present for the dashed curve.)

Neither type of amplifier — 3 or 4 stages — displays gain ripple over a 0 to 50° C temperature range as demonstrated by Figure 8. Variation of gain with temperature is roughly linear at any given in-band frequency. The intercept point for a three stage amplifier is +17 dBm and that of an amplifier with a balanced output stage is +25 dBm. Input and output VSWR's set by input and output isolators are better than 1.15:1 in-band. Power consumption of the three-stage amplifier is 0.5 watts — a third of the four stage amplifier value. A five stage 10 GHz amplifier, utilizing NEC 388's, with an input circuit designed in a similar fashion to the 14 GHz amplifier, had a noise figure of less than 2.95 dB over a 300 MHz bandwidth. Noise figure and gain versus frequency are shown in Figure 9. Gain is nominally 36.5 dB.
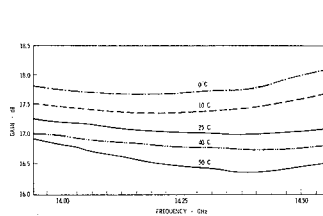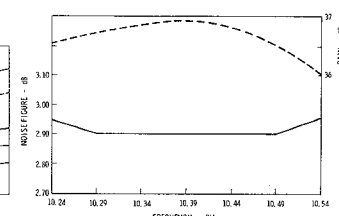
Conclusion

State-of-the-art noise figures have been achieved at 14 GHz by utilization of a narrow band design technique which enables one to match closely to Γ_{on} irrespective of changes in S-parameters amounting to less than 20° in angle or 20% in magnitude. This technique allows the designer to cascade single-ended circuits without concern for amplifier instability or gain ripple problems. Such a cascade is preferable over a balanced cascade to establish the lowest overall amplifier noise figure. The high processing yield of these modules indicates that low cost, easily productizable amplifiers can be built in this fashion.

Acknowledgements

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